



# PSMN3R3-80YSF

NextPower 80 V, 3.1 mOhm, 160 A, N-channel MOSFET in LFPAK56 package

30 August 2023

Preliminary data sheet

## 1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

## 2. Features and benefits

- Low  $Q_{rr}$  for higher efficiency and lower spiking
- 160 A  $I_D$  [max] – demonstrated continuous current rating
- Low  $Q_G \times R_{DSon}$  Figure of Merit (FOM) for high efficiency switching applications
- Strong avalanche energy rating ( $E_{as}$ )
- Avalanche rated and 100% tested
- Halogen free and RoHS compliant LFPAK56 package

## 3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in DC-DC
- Brushless DC (BLDC) motor control
- USB Power Delivery (PD) adapters
- Full-bridge and half-bridge applications
- Flyback and resonant topologies

## 4. Quick reference data

Table 1. Quick reference data

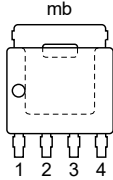
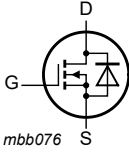
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	160	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	300	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>	-	2.5	3.1	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 105\text{ °C}$ ; <a href="#">Fig. 13</a>	-	4	5	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 40\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	5	15.5	34	nC
$Q_{G(tot)}$	total gate charge		36	72	108	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 49\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ Ω}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 113\text{ μs}$ ; <a href="#">Fig. 4</a>	[1]	-	289	mJ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 40\text{ V}$ ; <a href="#">Fig. 18</a>	-	36	-	nC

[1] Protected by 100% test

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R3-80YSF	LFAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R3-80YSF	3F3S80Y

## 8. Limiting values

Table 5. Limiting values

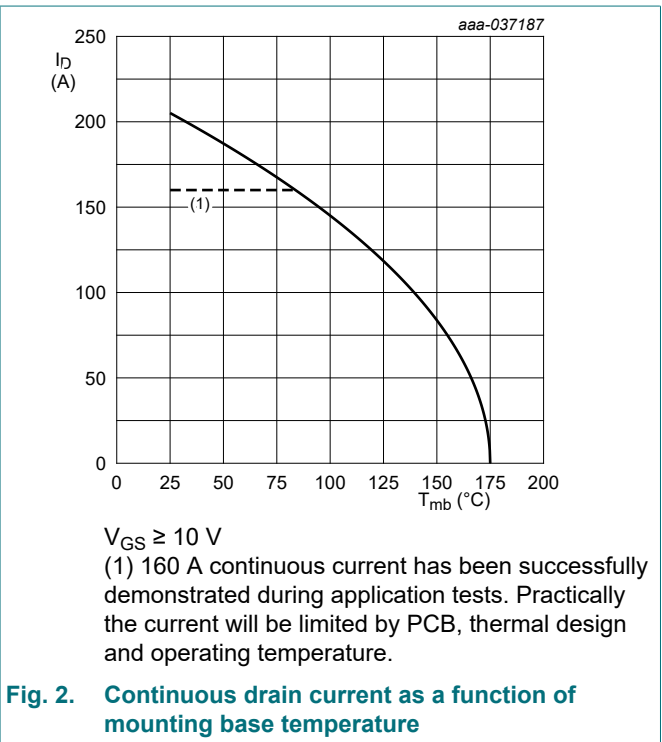
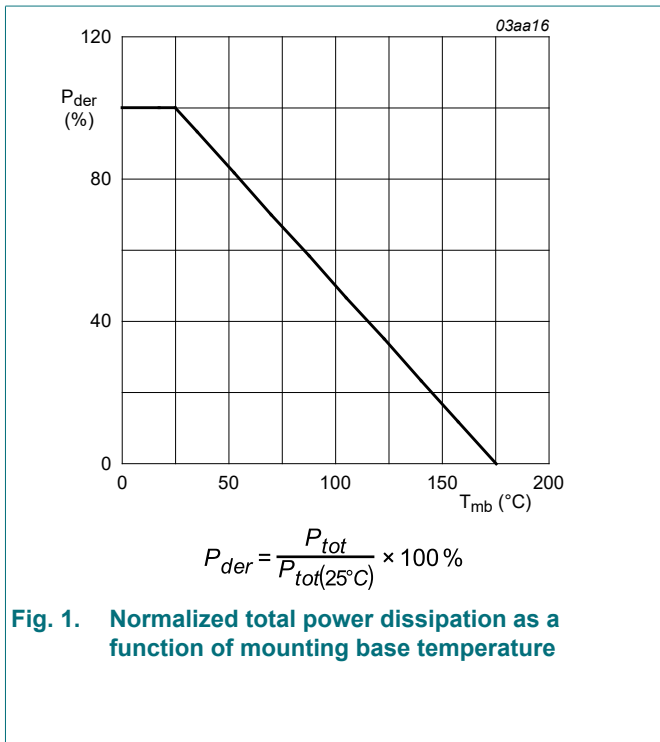
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ °C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	300	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	160	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>	-	145	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>	-	820	A
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C

NextPower 80 V, 3.1 mOhm, 160 A, N-channel MOSFET in LPAK56 package

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{\text{slid(M)}}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{\text{mb}} = 25\text{ °C}$	-	160	A
$I_{\text{SM}}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{\text{mb}} = 25\text{ °C}$	-	820	A
<b>Avalanche ruggedness</b>					
$E_{\text{DS(AL)S}}$	non-repetitive drain-source avalanche energy	$I_D = 49\text{ A}$ ; $V_{\text{sup}} \leq 80\text{ V}$ ; $R_{\text{GS}} = 50\text{ }\Omega$ ; $V_{\text{GS}} = 10\text{ V}$ ; $T_{\text{j(init)}} = 25\text{ °C}$ ; unclamped; $t_p = 113\text{ }\mu\text{s}$ ; Fig. 4	[1]	289	mJ
$I_{\text{AS}}$	non-repetitive avalanche current	$V_{\text{sup}} \leq 80\text{ V}$ ; $V_{\text{GS}} = 10\text{ V}$ ; $T_{\text{j(init)}} = 25\text{ °C}$ ; $R_{\text{GS}} = 50\text{ }\Omega$	[1]	49	A

[1] Protected by 100% test



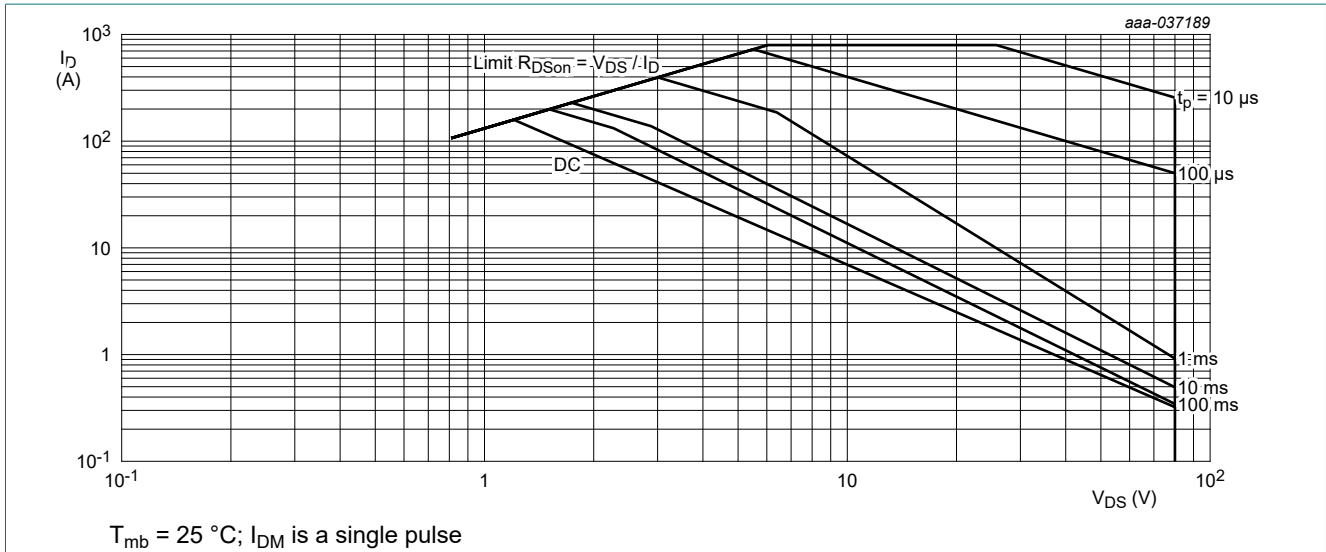


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

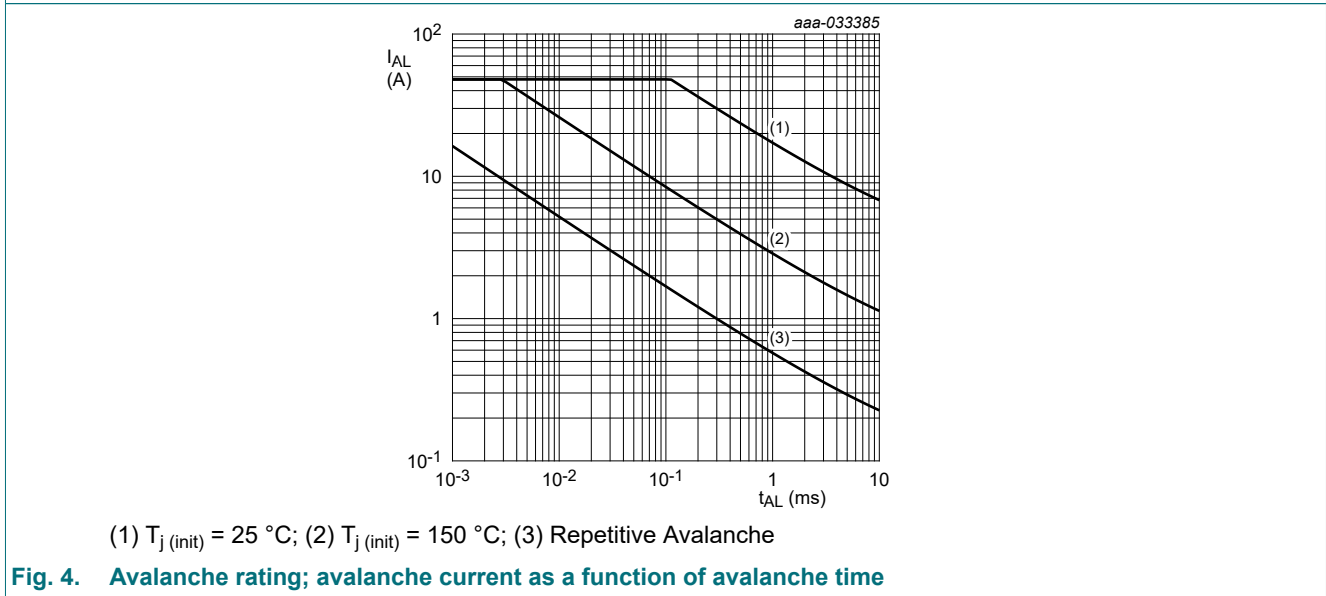


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	0.43	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 6</a>	-	42	-	K/W
		<a href="#">Fig. 7</a>	-	85	-	K/W

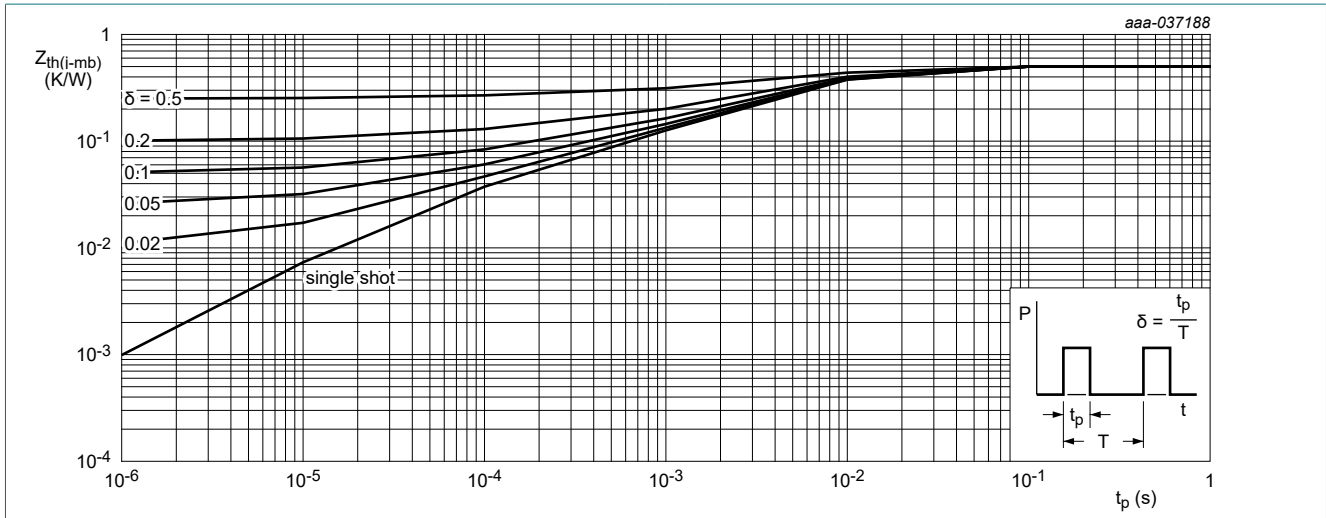


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

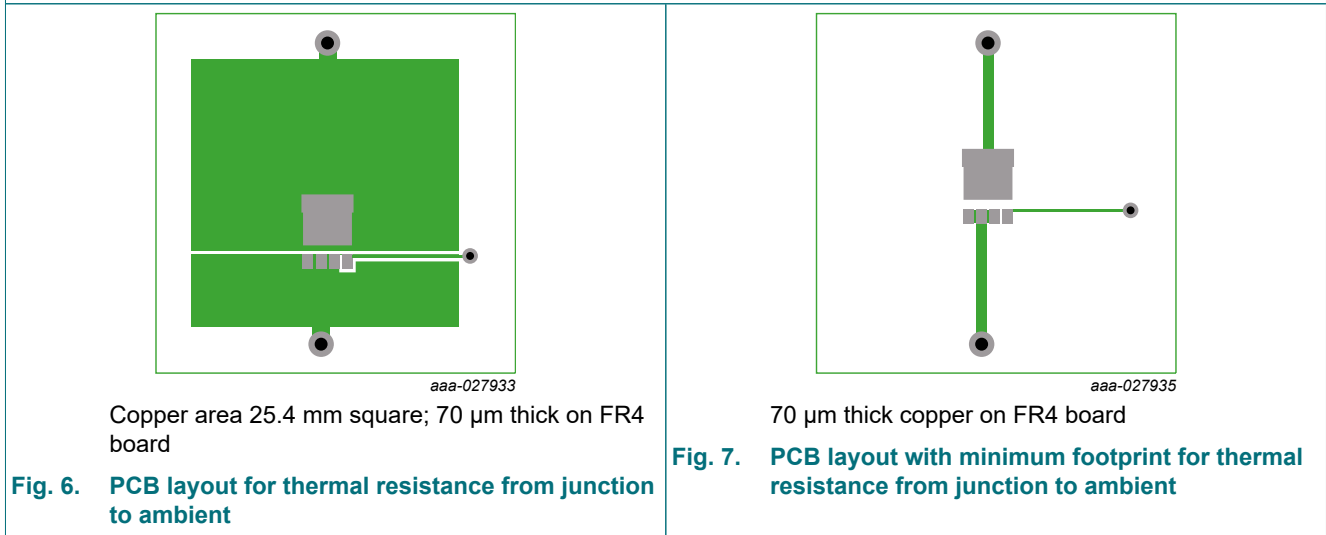


Fig. 6. PCB layout for thermal resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	89	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	85	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}$	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	2	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.4	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-7.8	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.07	1	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	2	100	μA
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

## NextPower 80 V, 3.1 mOhm, 160 A, N-channel MOSFET in LPAK56 package

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 12</a>	-	2.5	3.1	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 105 °C; <a href="#">Fig. 13</a>	-	4	5	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 13</a>	-	5.8	7.1	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>J</sub> = 25 °C	0.35	0.7	1.4	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	36	72	108	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	63	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	9	21.7	35	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	13.4	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	8.3	-	nC
Q <sub>GD</sub>	gate-drain charge		5	15.5	34	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 40 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	4.7	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>J</sub> = 25 °C; <a href="#">Fig. 16</a>	3000	4990	6986	pF
C <sub>oss</sub>	output capacitance		447	1420	1790	pF
C <sub>rss</sub>	reverse transfer capacitance		5	53	154	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 40 V; R <sub>L</sub> = 1.6 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω	-	20	-	ns
t <sub>r</sub>	rise time		-	19	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	38	-	ns
t <sub>f</sub>	fall time		-	22	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.81	1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 40 V; <a href="#">Fig. 18</a>	-	38	-	ns
Q <sub>r</sub>	recovered charge		-	36	-	nC

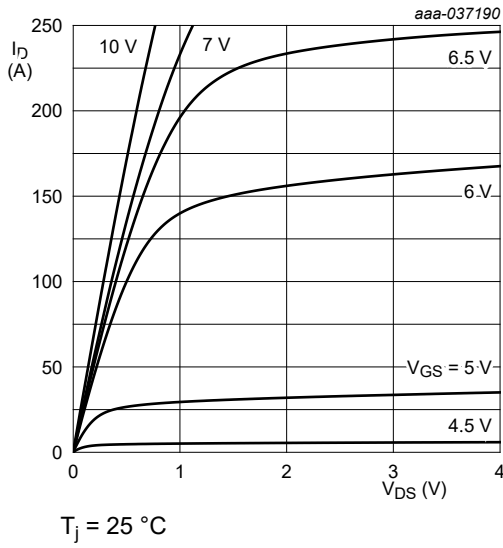


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

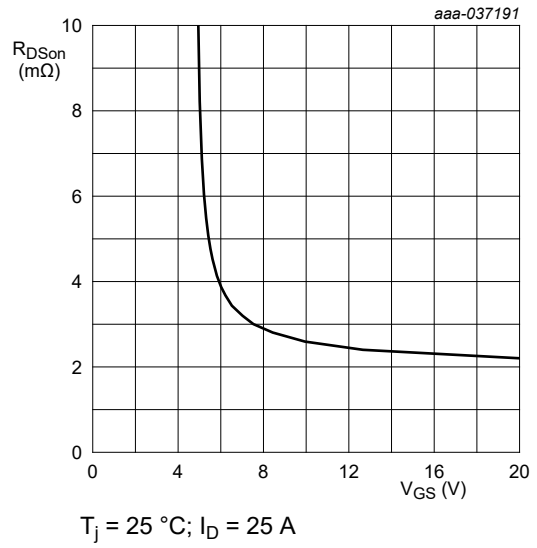


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

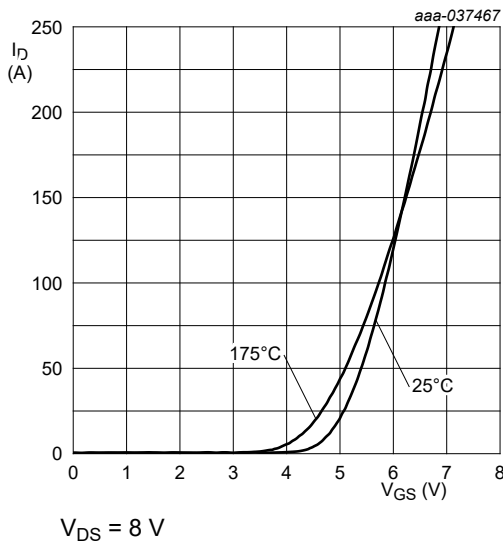


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

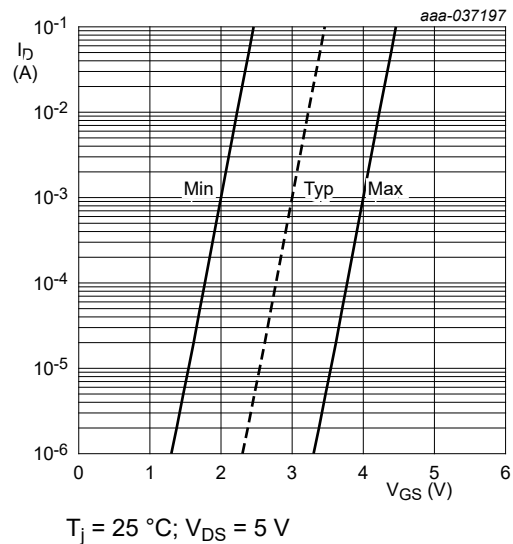


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

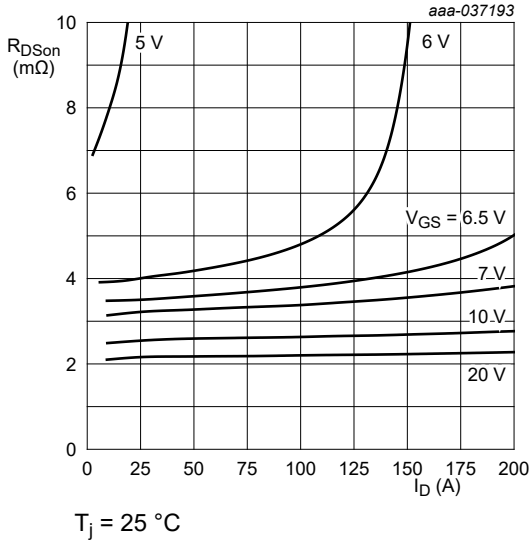
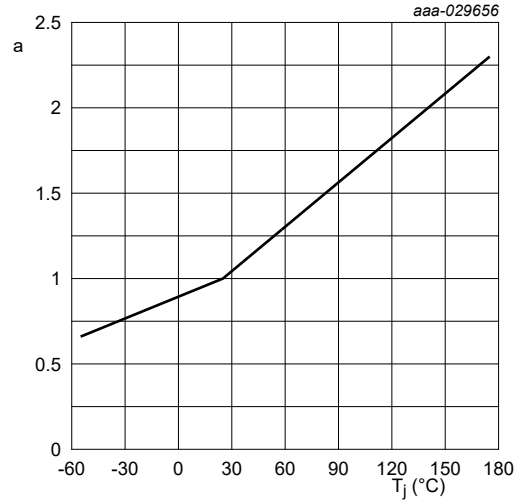


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

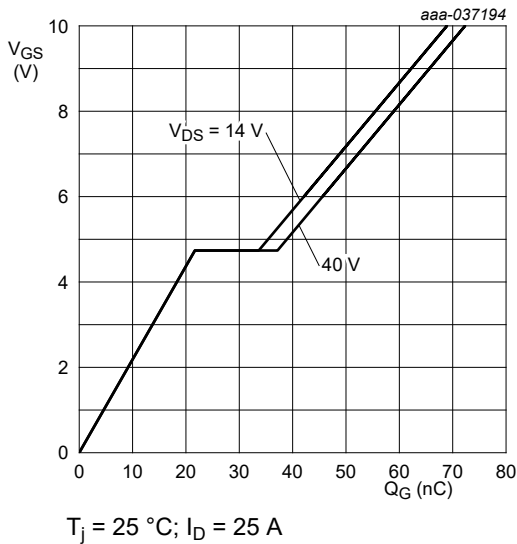


Fig. 14. Gate-source voltage as a function of gate charge; typical values

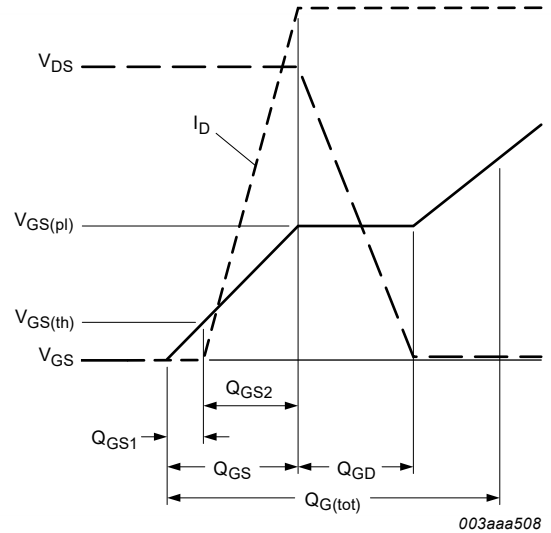


Fig. 15. Gate charge waveform definitions



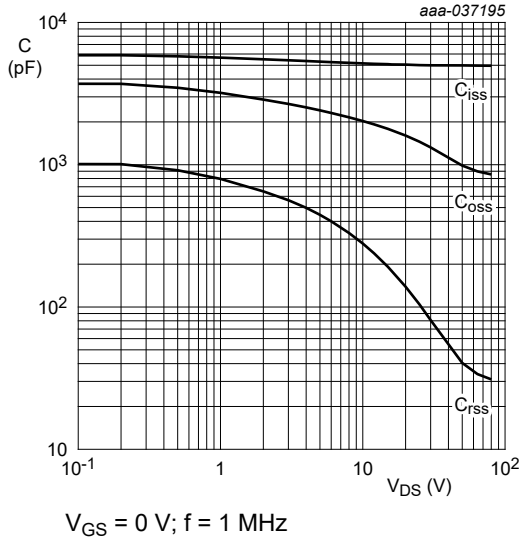


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

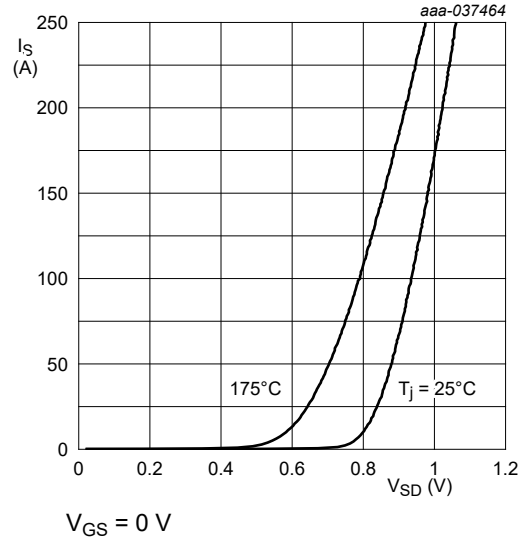


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

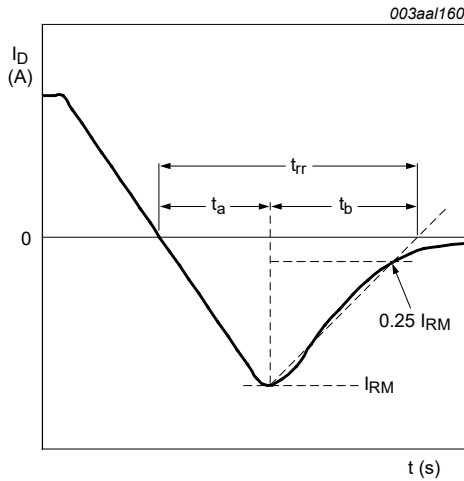


Fig. 18. Reverse recovery timing definition

### 11. Package outline

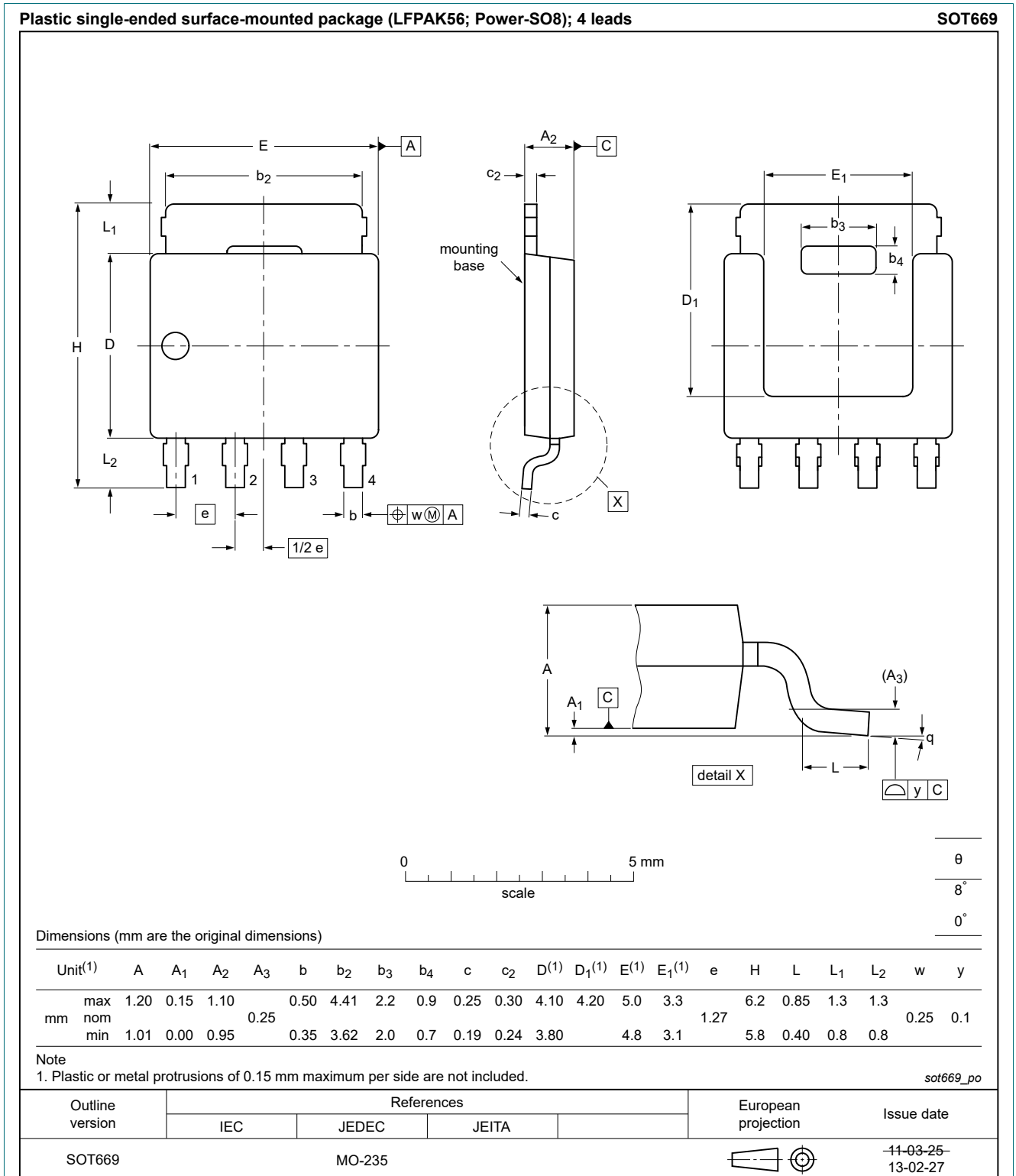


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Soldering

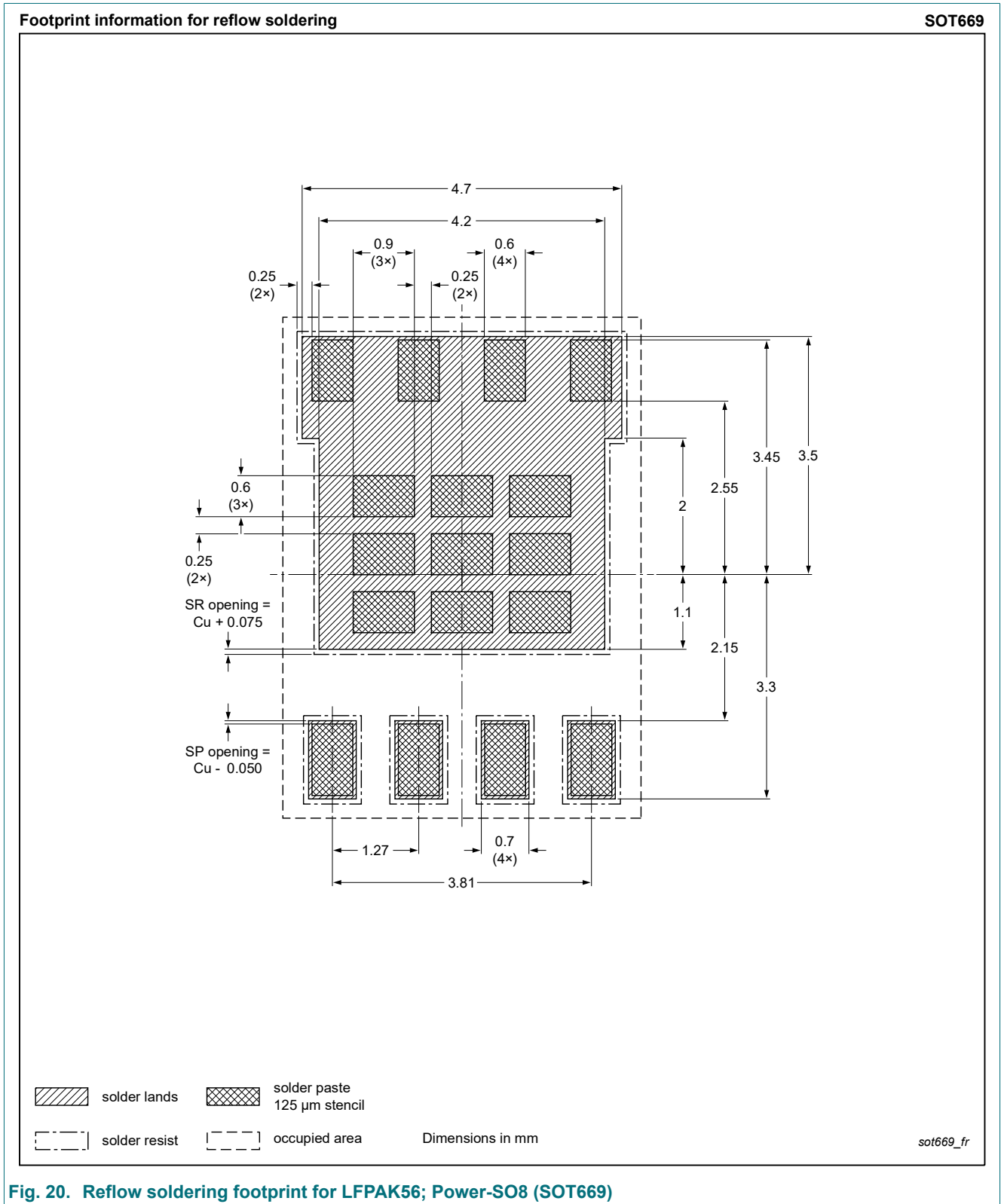
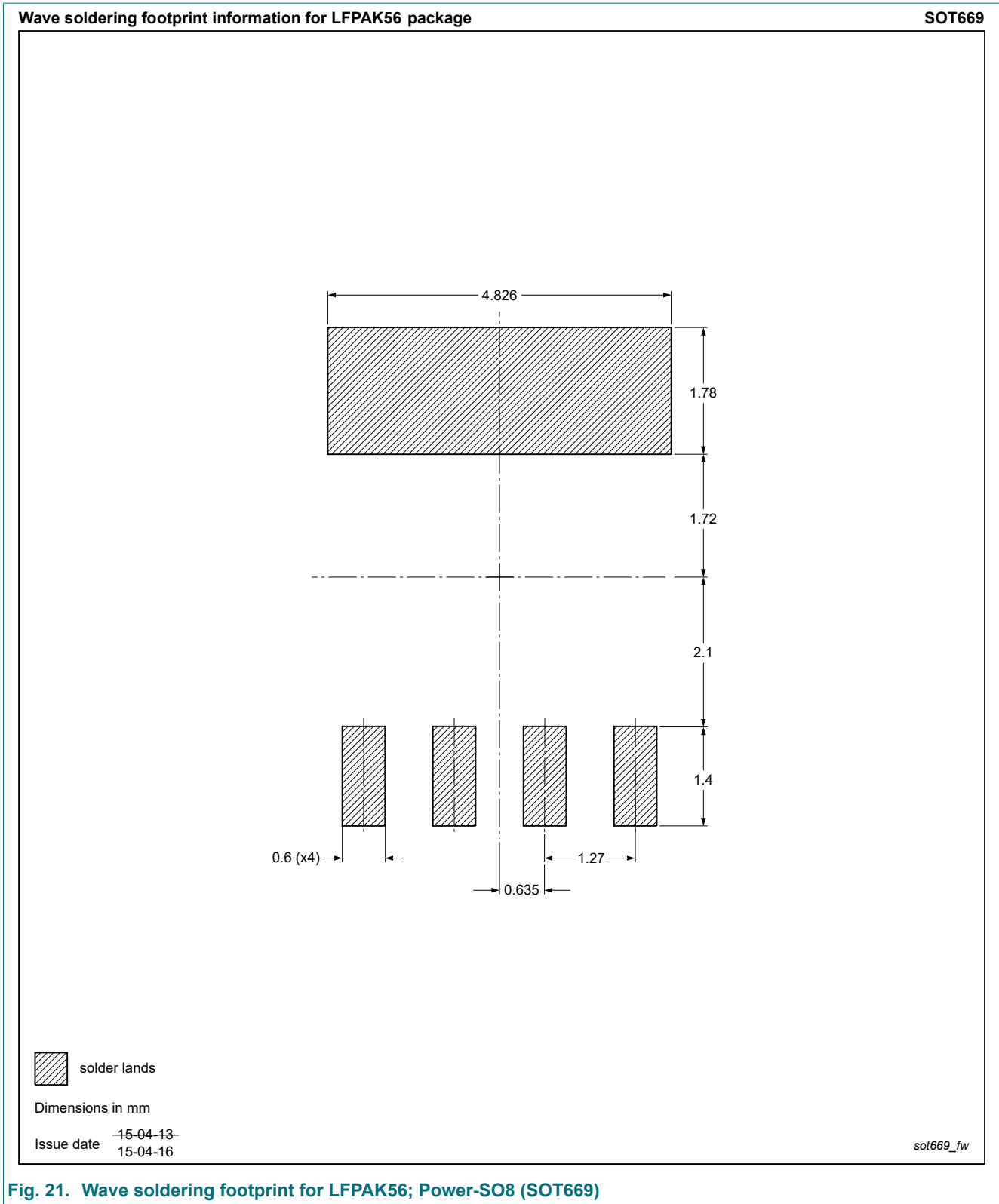


Fig. 20. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)



## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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